



**BUREAU
VERITAS**

Certificate of compliance

Applicant: SMA Solar Technology AG
Sonnenallee 1, 34266 Niestetal
Germany

Product: Photovoltaic (PV) inverter

Model: STP 125-70

Use in accordance with regulations:

Automatic disconnection device with three-phase mains surveillance in accordance with Engineering Recommendation G99/1-10 for photovoltaic systems with a three-phase parallel coupling via an inverter in the public mains supply. The automatic disconnection device is an integral part of the aforementioned inverter. This serves as a replacement for the disconnection device with isolating function, which can be accessed the distribution network provider at any time.

Applied rules and standards:

Engineering Recommendation G99/1-10:2024

Requirements for the connection of generation equipment in parallel with public distribution networks

Annex A – Type A Power Generating Modules

Annex B – Type B Power Generating Modules

Annex C – Type C Power Generating Modules

Annex D – Type D Power Generating Modules

DIN V VDE V 0126-1-1:2006 (4.1 Functional safety)

Automatic disconnection device between a generator and the public low-voltage grid

At the time of issue of this certificate the safety concept of an aforementioned representative product corresponds to the valid safety specifications for the specified use in accordance with regulations.

Report number: SGR-ESH-P24032185

Certificate number: U24-0895

Certification program: NSOP-0032-DEU-ZE-V10

Date of issue: 2024-09-13

Certification body



Certification body Bureau Veritas Consumer Products Services Germany GmbH accredited according to DIN EN ISO/IEC 17065

Testing laboratory accredited according to DIN EN ISO/IEC 17025

A partial representation of the certificate requires the written approval of Bureau Veritas Consumer Products Services Germany GmbH

Compliance Verification Report for Inverter Connected Power Generating Modules

Extract from test report according to the Engineering Recommendation G99

Nr. SGR-ESH-P24032185

Type Approval and declaration of compliance with the requirements of Engineering Recommendation G99.

PGM Technology:	Photovoltaic (PV) inverter		
Manufacturer / applicant:	SMA Solar Technology AG		
Address:	Sonnenallee 1, 34266 Niestetal Germany		
Tel	+49 561 9522-0	Fax:	+49 561 9522-100
Email:	Info@SMA.de	Website:	www.SMA.de

Rated values	STP 125-70	--	--	--
MPP DC voltage range [V]	180-1000	--	--	--
Max. input DC voltage [V]	1100	--	--	--
Max. input DC current [A]	12*30	--	--	--
Output AC voltage [V]	3L/N/PE, 230, 50/60Hz	--	--	--
Max. output AC current [A]	181,1	--	--	--
Output power [kVA]	125	--	--	--

Firmware version	4.0.0.R
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Note:

The tests were performed with firmware version 4.0.0.R changes in the firmware version on position 4.X.X have no effect on the required electrical properties. "X" could be any number (or sign) higher (newer) than the tested version.

Description of the structure of the power generation unit:

The power generation unit is equipped with a PV and line-side EMC filter. The power generation unit has no galvanic isolation between DC input and AC output. Output switch-off is performed with single-fault tolerance based on two series-connected relays in (each) line and neutral. This enables a safe disconnection of the power generation unit from the network in case of error.

The above stated Generating Units are tested according the requirements in the Engineering Recommendation G99/1-10. Any modification that affects the stated tests must be named by the manufacturer/supplier of the product to ensure that the product meets all requirements of the Engineering Recommendation G99/1-10.

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Operating Range.

Test 1	Voltage = 85% of nominal (195,5V) Frequency = 47Hz Power Factor = 1 Period of test 20 s
Connection:	Always connected
Limit:	Always connected
Test 2	Voltage = 85% of nominal (195,5V) Frequency = 47,5Hz Power Factor = 1 Period of test 90 minutes
Connection:	Always connected
Limit:	Always connected
Test 3	Voltage = 110% of nominal (253V) Frequency = 51,5Hz Power Factor = 1 Period of test 90 minutes
Connection:	Always connected
Limit:	Always connected
Test 4	Voltage = 110% of nominal (253V) Frequency = 52,0Hz Power Factor = 1 Period of test 15 minutes
Connection:	Always connected
Limit:	Always connected
Test 5	Voltage = 100% of nominal (230 V) Frequency = 50,0 Hz Power Factor = 1 Period of test 90 minutes
Connection:	Always connected
Limit:	Always connected
Test 6	Confirm that the Power Generating Module is capable of staying connected to the Distribution Network and operate at rates of change of frequency up to 1 Hzs-1 as measured over a period of 500ms. Note that this is not expected to be demonstrated on site.
Connection:	Always connected
Limit:	Always connected

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Protection. Voltage tests.

Phase 1

Function	Setting		Trip test		No trip test	
	Voltage [V]	Time delay [s]	Voltage [V]	Time delay [s]	Voltage / time	Confirm no trip
U/V	184	2,5	184,2	2,547	188V / 5,0s	No trip
					180V / 2,45s	No trip
O/V stage 1	262,2	1,0	262,3	1,047	258,2V 5,0s	No trip
O/V stage 2	273,7	0,5	273,8	0,513	269,7V 0,95s	No trip
					277,7V 0,45s	No trip

Protection. Voltage tests.

Phase 2

Function	Setting		Trip test		No trip test	
	Voltage [V]	Time delay [s]	Voltage [V]	Time delay [s]	Voltage / time	Confirm no trip
U/V	184	2,5	184,2	2,542	188V / 5,0s	No trip
					180V / 2,45s	No trip
O/V stage 1	262,2	1,0	262,3	1,052	258,2V 5,0s	No trip
O/V stage 2	273,7	0,5	273,8	0,524	269,7V 0,95s	No trip
					277,7V 0,45s	No trip

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Protection. Voltage tests.

Phase 3

Function	Setting		Trip test		No trip test	
	Voltage [V]	Time delay [s]	Voltage [V]	Time delay [s]	Voltage / time	Confirm no trip
U/V	184	2,5	184,2	2,537	188V / 5,0s	No trip
					180V / 2,45s	No trip
O/V stage 1	262,2	1,0	262,3	1,039	258,2V 5,0s	No trip
O/V stage 2	273,7	0,5	273,8	0,521	269,7V 0,95s	No trip
					277,7V 0,45s	No trip

Note. For Voltage tests the Voltage required to trip is the setting $\pm 3,45V$. The time delay can be measured at a larger deviation than the minimum required to operate the protection. The No trip tests need to be carried out at the setting $\pm 4V$ and for the relevant times as shown in the table above to ensure that the protection will not trip in error.

Protection. Frequency tests.

Function	Setting		Trip test		No trip test	
	Frequency [Hz]	Time delay [s]	Frequency [Hz]	Time delay [s]	Frequency / time	Confirm no trip
U/F stage 1	47,5	20	49,50	20,023	47,7Hz / 30s	No trip
U/F stage 2	47	0,5	47,00	0,520	47,2Hz / 19,5s	No trip
					46,8Hz / 0,45s	No trip
O/F stage 2	52	0,5	52,00	k0,529	51,8Hz / 120s	No trip
					52,2Hz / 0,45s	No trip

Note. For Frequency Trip tests the Frequency required to trip is the setting $\pm 0,1Hz$. In order to measure the time delay a larger deviation than the minimum required to operate the projection can be used. The "No-trip tests" need to be carried out at the setting $\pm 0,2Hz$ and for the relevant times as shown in the table above to ensure that the protection will not trip in error.

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Protection. Loss of Mains.

Inverters tested according to BS EN 62116.

Balancing load on islanded network	33% of -5% Q Test 22	66% of -5% Q Test 12	100% of -5% P Test 5	33% of +5% Q Test 31	66% of +5% Q Test 21	100% of +5% P Test 10
Trip time. Ph1 fuse removed [s]	114	142	179	144	169	212

Note. Trip time limit is 0,5s.

Protection. Re-connection timer.

Test should prove that the reconnection sequence starts in no less than 20 seconds for restoration of voltage and frequency to within the stage 1 settings of table 10.1.

Over Voltage (188,0 V)				
Time delay setting		Measured delay		
20s		78,1		
Under Voltage (258,2 V)				
Time delay setting		Measured delay		
20s		78,1		
Over Frequency (51,9 Hz)				
Time delay setting		Measured delay		
20s		78,1		
Under Frequency (47,5 Hz)				
Time delay setting		Measured delay		
20s		78,1		
	Checks on no reconnection when voltage or frequency is brought to just outside stage 1 limits of table 1.			
	At 266,2V	At 180,0V	At 47,4Hz	At 52,1Hz
Confirmation that the Generating Unit does not re-connect.	No reconnection	No reconnection	No reconnection	No reconnection

Protection. Frequency change, Stability test.

	Start Frequency [Hz]	Change	Test Duration	Confirm no trip
Positive Vector Shift	49,5	+50 degrees		No trip
Negative Vector Shift	50,5	-50 degrees		No trip
Positive Frequency drift	49,0 to 51,0	+0,95Hz/sec	2,1s	No trip
Negative Frequency drift	51,0 to 49,0	-0,95Hz/sec	2,1s	No trip

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Limited Frequency Sensitive Mode – Over Frequency

1-min mean value [Hz]:	a) 50,00	b) 50,45	c) 50,70	d) 51,15	e) 50,70	f) 50,45	g) 50,00
1. Measurement a) to g): Active power output > 80% P_n							
Frequency [Hz]:	50,00	50,45	50,70	51,15	50,70	50,45	50,00
P_{expected} [kW]:	125,00	123,75	117,50	106,25	117,50	123,75	125,00
P_{measured} [kW]:	124,06	122,93	116,84	105,80	116,84	122,91	124,03
2. Measurement a) to g): Active power output 40% and 60% P_n							
Frequency [Hz]:	50,00	50,45	50,70	51,15	50,70	50,45	50,00
P_{expected} [kW]:	62,50	61,25	55,00	43,75	55,00	61,25	62,50
P_{measured} [kW]:	62,23	61,10	54,89	43,12	54,65	60,77	62,02

Output Power with falling Frequency

Frequency setpoint [Hz]:	50,00	49,50	49,00	48,00	47,60	47,10
Frequency [Hz]:	50,00	49,50	49,00	48,00	47,60	47,1
Active power [kW]:	124,48	124,48	124,49	124,48	124,48	124,49
ΔP/P_{max} [%]:	0,42	0,42	0,41	0,41	0,42	0,40

Note.

No Power reduction takes place for electronic inverter

Compliance Verification Report for Inverter Connected Power Generating Modules

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Power Quality. Harmonics.

Phase 1						
SSEG rating per phase (rpp)			STP 125-70			
	At 45-55% of rated output 20,83 kW		100% of rated output 41,67 kW			
Harmonic	Measured Value (MV) in [A]	Measured Value (%) in [A]	Measured Value (MV) in [A]	Measured Value (%) in [A]	Limit in BS EN61000-3-2 in Amps	Higher limit for odd harmonics 21 and above
2nd	0,064	0,035	0,121	0,067	1,080	
3rd	0,215	0,119	0,112	0,062	2,300	
4th	0,087	0,048	0,103	0,057	0,430	
5th	0,095	0,052	3,200	1,767	1,140	
6th	0,084	0,047	0,094	0,052	0,300	
7th	0,358	0,198	1,835	1,013	0,770	
8th	0,063	0,035	0,137	0,076	0,230	
9th	0,088	0,049	0,193	0,106	0,400	
10th	0,095	0,053	0,166	0,092	0,184	
11th	0,080	0,044	0,972	0,537	0,330	
12th	0,073	0,040	0,090	0,050	0,153	
13th	0,201	0,111	1,728	0,954	0,210	
14th	0,039	0,021	0,088	0,048	0,131	
15th	0,345	0,190	0,167	0,092	0,150	
16th	0,061	0,034	0,115	0,063	0,115	
17th	0,067	0,037	0,420	0,232	0,132	
18th	0,062	0,034	0,066	0,036	0,102	
19th	0,275	0,152	1,357	0,749	0,118	
20th	0,037	0,021	0,097	0,054	0,092	
21th	0,250	0,138	0,164	0,091	0,107	0,160
22th	0,044	0,024	0,093	0,051	0,084	
23th	0,046	0,025	0,757	0,418	0,098	0,147
24th	0,034	0,019	0,059	0,033	0,077	
25th	0,064	0,035	0,764	0,422	0,090	0,135
26th	0,215	0,119	0,099	0,055	0,071	
27th	0,087	0,048	0,059	0,032	0,083	0,124
28th	0,095	0,052	0,069	0,038	0,066	
29th	0,084	0,047	0,364	0,201	0,078	0,117
30th	0,358	0,198	0,049	0,027	0,061	
31th	0,063	0,035	0,204	0,113	0,073	0,109
32th	0,088	0,049	0,058	0,032	0,058	
33th	0,095	0,053	0,045	0,025	0,068	0,102
34th	0,080	0,044	0,047	0,026	0,054	
35th	0,073	0,040	0,094	0,052	0,064	0,096
36th	0,201	0,111	0,041	0,023	0,051	
37th	0,039	0,021	0,128	0,070	0,061	0,091
38th	0,345	0,190	0,062	0,034	0,048	
39th	0,061	0,034	0,031	0,017	0,058	0,087
40th	0,067	0,037	0,029	0,016	0,046	
THD40	--	1,613	--	2,541	23%	13%
PWHD	--	2,341	--	4,772	23%	22%

Note the higher limits for odd harmonics 21 and above are only allowable under certain conditions, if these higher limits are utilised please state the exemption used as detailed in part 6.2.3.4 of BS EN 61000-3-2 in the box below.

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Power Quality. Harmonics.

Phase 2

Generating Unit rating per phase (rpp)			STP 125-70			
	At 45-55% of rated output 20,83 kW		100% of rated output 41,67 kW			
Harmonic	Measured Value (MV) in [A]	Measured Value (MV) in [%]	Measured Value (MV) in [A]	Measured Value (MV) in [%]	Limit in BS EN61000-3-12 in %	
					1 phase	3 phase
2nd	0,051	0,028	0,276	0,152	8%	8%
3rd	0,172	0,095	0,348	0,192	21,6%	N/A
4th	0,103	0,057	0,060	0,033	4%	4%
5th	0,120	0,066	3,210	1,772	10,7%	10,7%
6th	0,111	0,061	0,070	0,039	2,67%	2,67%
7th	0,358	0,197	1,986	1,096	7,2%	7,2%
8th	0,056	0,031	0,127	0,070	2%	2%
9th	0,107	0,059	0,091	0,050	3,8%	N/A
10th	0,088	0,048	0,114	0,063	1,6%	1,6%
11th	0,076	0,042	0,904	0,499	3,1%	3,1%
12th	0,069	0,038	0,084	0,046	1,33%	1,33%
13th	0,236	0,130	1,792	0,989	2%	2%
14th	0,041	0,023	0,094	0,052	N/A	N/A
15th	0,367	0,203	0,078	0,043	N/A	N/A
16th	0,055	0,030	0,126	0,070	N/A	N/A
17th	0,049	0,027	0,532	0,294	N/A	N/A
18th	0,057	0,032	0,066	0,036	N/A	N/A
19th	0,236	0,130	1,527	0,843	N/A	N/A
20th	0,038	0,021	0,068	0,037	N/A	N/A
21th	0,234	0,129	0,123	0,068	N/A	N/A
22th	0,041	0,023	0,122	0,068	N/A	N/A
23th	0,045	0,025	0,618	0,341	N/A	N/A
24th	0,053	0,029	0,055	0,030	N/A	N/A
25th	0,051	0,028	0,724	0,400	N/A	N/A
26th	0,172	0,095	0,108	0,059	N/A	N/A
27th	0,103	0,057	0,057	0,032	N/A	N/A
28th	0,120	0,066	0,076	0,042	N/A	N/A
29th	0,111	0,061	0,407	0,225	N/A	N/A
30th	0,358	0,197	0,047	0,026	N/A	N/A
31th	0,056	0,031	0,160	0,088	N/A	N/A
32th	0,107	0,059	0,053	0,030	N/A	N/A
33th	0,088	0,048	0,037	0,020	N/A	N/A
34th	0,076	0,042	0,040	0,022	N/A	N/A
35th	0,069	0,038	0,132	0,073	N/A	N/A
36th	0,236	0,130	0,030	0,017	N/A	N/A
37th	0,041	0,023	0,129	0,071	N/A	N/A
38th	0,367	0,203	0,066	0,037	N/A	N/A
39th	0,055	0,030	0,063	0,035	N/A	N/A
40th	0,049	0,027	0,041	0,023	N/A	N/A
THD ₄₀ [%]	--	1,605	--	2,612	23%	13%
PWHD [%]	--	2,286	--	4,950	23%	22%

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Power Quality. Harmonics.

Phase 3						
Generating Unit rating per phase (rpp)			STP 125-70			
	At 45-55% of rated output 20,83 kW		100% of rated output 41,67 kW			
Harmonic	Measured Value (MV) in [A]	Measured Value (MV) in [%]	Measured Value (MV) in [A]	Measured Value (MV) in [%]	Limit in BS EN61000-3-12 in %	
					1 phase	3 phase
2nd	0,122	0,068	0,215	0,119	8%	8%
3rd	0,153	0,084	0,315	0,174	21,6%	N/A
4th	0,105	0,058	0,089	0,049	4%	4%
5th	1,531	0,845	3,225	1,780	10,7%	10,7%
6th	0,102	0,056	0,070	0,039	2,67%	2,67%
7th	1,858	1,026	1,862	1,028	7,2%	7,2%
8th	0,071	0,039	0,076	0,042	2%	2%
9th	0,169	0,094	0,217	0,120	3,8%	N/A
10th	0,078	0,043	0,131	0,073	1,6%	1,6%
11th	0,299	0,165	0,822	0,454	3,1%	3,1%
12th	0,063	0,035	0,062	0,034	1,33%	1,33%
13th	1,208	0,667	1,749	0,966	2%	2%
14th	0,058	0,032	0,098	0,054	N/A	N/A
15th	0,075	0,041	0,224	0,124	N/A	N/A
16th	0,096	0,053	0,086	0,047	N/A	N/A
17th	0,310	0,171	0,499	0,275	N/A	N/A
18th	0,064	0,035	0,059	0,033	N/A	N/A
19th	0,196	0,108	1,468	0,810	N/A	N/A
20th	0,112	0,062	0,091	0,051	N/A	N/A
21th	0,161	0,089	0,281	0,155	N/A	N/A
22th	0,100	0,055	0,086	0,047	N/A	N/A
23th	0,294	0,162	0,704	0,389	N/A	N/A
24th	0,064	0,035	0,049	0,027	N/A	N/A
25th	0,083	0,046	0,666	0,368	N/A	N/A
26th	0,103	0,057	0,096	0,053	N/A	N/A
27th	0,081	0,045	0,086	0,047	N/A	N/A
28th	0,076	0,042	0,057	0,031	N/A	N/A
29th	0,209	0,115	0,363	0,200	N/A	N/A
30th	0,038	0,021	0,036	0,020	N/A	N/A
31th	0,352	0,194	0,227	0,125	N/A	N/A
32th	0,055	0,030	0,063	0,035	N/A	N/A
33th	0,084	0,046	0,053	0,029	N/A	N/A
34th	0,044	0,024	0,055	0,030	N/A	N/A
35th	0,236	0,131	0,165	0,091	N/A	N/A
36th	0,036	0,020	0,032	0,018	N/A	N/A
37th	0,262	0,145	0,121	0,067	N/A	N/A
38th	0,043	0,024	0,030	0,017	N/A	N/A
39th	0,045	0,025	0,072	0,040	N/A	N/A
40th	0,057	0,031	0,038	0,021	N/A	N/A
THD ₄₀ [%]	--	1,570	--	2,566	23%	13%
PWHD [%]	--	2,273	--	4,904	23%	22%

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Nr. SGR-ESH-P24032185

Power Quality. Power factor.

Output power	216,2V	230V	253V	Measured at three voltage levels and at full output. Voltage to be maintained within $\pm 1,5\%$ of the stated level during the test.
20%	0,9985	0,9987	0,9986	
50%	0,9994	0,9995	0,9997	
75%	0,9993	0,9995	0,9997	
100%	0,9994	0,9996	0,9998	
Limit	>0,95	>0,95	>0,95	

Power Quality. Voltage fluctuation and Flicker.

	Starting			Stopping			Running	
	dmax	dc	d(t)	dmax	dc	d(t)	Pst	Plt 2 hours
Measured values at test impedance	0,55	0	0	0,55	0	0	0,09	0,07
Measured values at standard impedance	0,55	0	0	0,55	0	0	0,09	0,07
Values for maximum impedance	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Limits set under BS EN 61000-3-11	4%	3,3%	3,3% 500ms	4%	3,3%	3,3% 500ms	1,0	0,65
Test impedance	R	0,24* 0,4^	Ω	XI	0,15* 0,25	Ω		
	Z		Ω					
Standard impedance	R	0,24* 0,4^	Ω	XI	0,15* 0,25^	Ω		
	Z		Ω					
Maximum impedance	R	0,24* 0,4^	Ω	XI	0,15* 0,25^	Ω		
	Zmax		Ω					

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Power Quality. DC injection.

Phase 1

Test level power [%]	10	55	100
Recorded value [mA]	278,0	338,5	313,9
Recorded value [%]	0,15	0,19	0,17
Limit [%]	0,25	0,25	0,25

Phase 2

Test level power [%]	10	55	100
Recorded value [mA]	175,9	261,1	377,8
Recorded value [%]	0,10	0,14	0,21
Limit [%]	0,25	0,25	0,25

Phase 3

Test level power [%]	10	55	100
Recorded value [mA]	90,5	259,6	258,2
Recorded value [%]	0,05	0,14	0,14
Limit [%]	0,25	0,25	0,25

Note. Informative measurement of DC-injection of each phase of the inverter and a limit of 0,25% per phase of the rated current per phase as pass criteria.

Sum of all Phases

Tests are carried out at three defined power levels $\pm 5\%$. At 230 V a 125 kW three phase Inverter has a current output of 543,5 A so DC limit is 1359 mA. These tests is undertaken in accordance with Annex A.7.1.4.4.

The % DC injection ("as % of rated AC current" below) is calculated as follows:

% DC injection = Recorded DC value in Amps / Base current where the base current is the Registered Capacity (W) / V phase.

The % DC injection should not be greater than 0,25%.

Sum of all Phases

Test level power [%]	10	55	100
Recorded value [mA]	544,4	859,2	949,9
Recorded value [%]	0,10	0,16	0,17
Limit [%]	0,25	0,25	0,25

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Fault level Contribution.

Phase 1

For a directly coupled SSEG			For a Inverter SSEG		
Parameter	Symbol	Value	Time after fault	Volts [V]	Amps [A]
Peak Short Circuit current	I_p	N/A	20ms	27,6	131,7
Initial Value of aperiodic current	A	N/A	100ms	14,0	64,4
Initial symmetrical short-circuit current*	I_k	N/A	250ms	10,7	46,4
Decaying (aperiodic) component of short circuit current*	i_{DC}	N/A	500ms	9,4	38,6
Reactance/Resistance Ratio of source*	X/R	N/A	Time to Trip [s]	0,577	

Phase 2

For a directly coupled SSEG			For a Inverter SSEG		
Parameter	Symbol	Value	Time after fault	Volts [V]	Amps [A]
Peak Short Circuit current	I_p	N/A	20ms	79,5	162,3
Initial Value of aperiodic current	A	N/A	100ms	36,2	76,5
Initial symmetrical short-circuit current*	I_k	N/A	250ms	23,6	53,2
Decaying (aperiodic) component of short circuit current*	i_{DC}	N/A	500ms	17,6	42,7
Reactance/Resistance Ratio of source*	X/R	N/A	Time to Trip [s]	0,573	

Phase 3

For a directly coupled SSEG			For a Inverter SSEG		
Parameter	Symbol	Value	Time after fault	Volts [V]	Amps [A]
Peak Short Circuit current	I_p	N/A	20ms	58,4	145,1
Initial Value of aperiodic current	A	N/A	100ms	27,0	69,7
Initial symmetrical short-circuit current*	I_k	N/A	250ms	18,1	49,1
Decaying (aperiodic) component of short circuit current*	i_{DC}	N/A	500ms	14,0	40,0
Reactance/Resistance Ratio of source*	X/R	N/A	Time to Trip [s]	0,563	

For rotating machines and linear piston machines the test should produce a 0s – 2s plot of the short circuit current as seen at the Generating Unit terminals.

* Values for these parameters should be provided where the short circuit duration is sufficiently long to enable interpolation of the plot.

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Self Monitoring – Solid state switching.	N/A
It has been verified that in the event of the solid state switching device failing to disconnect the Power Park Module, the voltage on the output side of the switching device is reduced to a value below 50 volts within 0,5 seconds.	N/A
Note. Unit do not provide solid state switching relays. In case the semiconductor bridge is switched off, then the voltage on the output drops to 0. In this case the relays on the output will also open (Functional safety of the internal automatic disconnection device according to VDE 0126-1-1 / VDE 0124-100).	

Cyber security	P
Confirm that the Manufacturer or Installer of the Micro-generator has provided a statement describing how the Micro-generator has been designed to comply with cyber security requirements, as detailed in 9.7.	Yes
Note. Different levels of access, all are password protected, only certain parameters can be changed on maintenance level.	

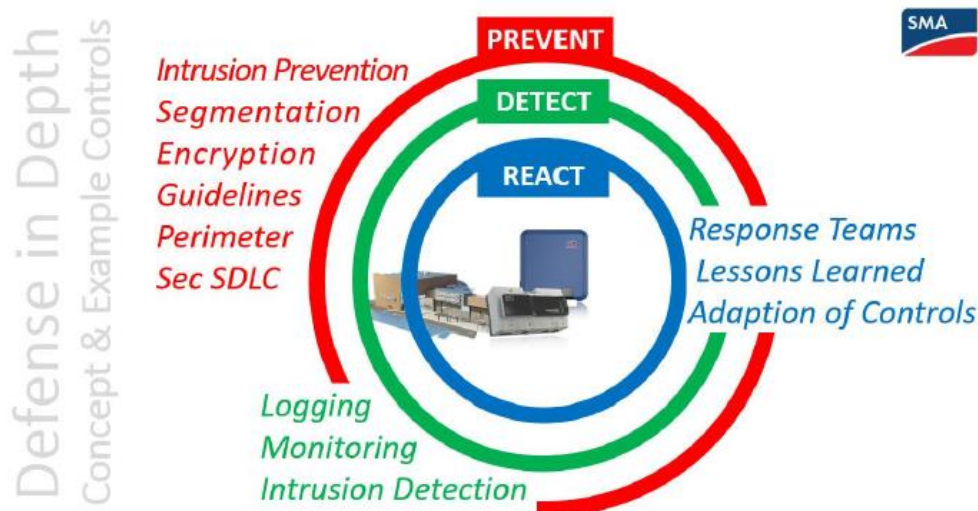
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1 Overall Cyber Security Concept

SMA's Secure Development Life Cycle is integrated in a holistic cyber security concept to achieve an appropriate level of security not only for our devices itself but also for the overall systems integrating SMA devices. An overview of this concept can be depicted by the following figure:



1.1 Main Steps in SMA's SDLC



Implementation of a SDLC is an important measure to achieve the goal of high level cyber security. SMA's controls and measures for each step are described in next paragraph.

1.2 Conformity Assessment for EN 303 645

SMA has launched an internal project to verify the conformity of products with the cyber security standard EN 303645. A manufacturer's declaration of conformity is planned for mid-2024.

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2 Controls and Measures

SMA ensures the implementation and application of the following controls and measures:

2.1 SDLC, Step 1: Threat Modeling and Risk Assessment

- Regular threat modeling and risk assessments for new products and product releases:
 - Identifying all relevant assets and trust boundaries
 - Describing data flows
 - Analyzing corresponding threats based on a standard procedure (STRIDE)
- Determination of related risks based on a standard model (OWASP Risk Rating Model)
- Definition of treatment for identified risks

2.2 SDLC, Step 2: Requirement Engineering

- Collection and prioritization of mitigating measures based on identified risk level
- Creation of implementation tickets for
 - Addressing measures and controls
 - Tracking of implementation state
- Secure updateability of every device
As a foundation for assuring security of devices in the field
 - Updates can be performed manually or automatically

2.3 SDLC, Step 3: Secure Coding

- Provision of mandatory requirements by SMA's *Cyber Security Products Directive*
Comprising >100 organizational and technical requirements for product development
- Code reviews by 4-eyes principle for security relevant code
- Automated Static Code Analysis (Build Pipeline)

2.4 SDLC, Step 4: Release, Production and Operation

- SBOM generation and vulnerability scan for 3rd party Components (Build Pipeline) for ennexOS-based products
- Extended device, system and field test procedures
- Provision of secure update mechanisms
Integrity- and authenticity checks by signing of firmware packages
- Secure service-level access (locally and remotely)
Based on owner/operator consent to service-access and 2-factor authentication of service users

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2.5 SDLC, Step 5: Incident Response

- Product Security Incident Response Process in place
Process management by dedicated Product Security Incident Response Team
- Information on responsible disclosure on SMA Website ([LINK](#))
Disclosed vulnerabilities are acknowledged within 3 working days and acted on within a pre-defined period of time depending on the corresponding risk assessment.
- Membership at CERT@VDE ([LINK](#)) for support of coordinated disclosure process

2.6 SDLC, Step 6: End-of-Life (EOL) and Decommissioning

- For decommissioning factory reset including deletion of sensitive data
- Optional secure disposal of devices at SMA

2.7 SDLC, Complementary Measures (A): Awareness

- Regular cyber security trainings for SMA employees
- Documentation of secure operation for installers and system operators
- Collaboration in international bodies as e.g. CEN/CENELEC, DIN, OWASP, SunSpec, VDE
- Specific Cyber Security Innovation Working Group
Expert board controlling and evaluating upcoming technologies and threats regarding Cyber Security; Initiation of technology projects; Regular steering board meetings once a month

2.8 SDLC, Complementary Measures (B): Generic Security Measures

- The model designation of products is accessible via the device's nameplate
- System hardening: Only necessary functions and services are enabled
- Communication between the considered device and other devices is secured (encrypted, authenticated, integrity protected)
where applicable and technically feasible regarding interoperability and intended use
- Storing sensitive data securely
- State-of-the-art password policy in use
- Obligation to change default passwords during commissioning
- Brute-force protecting measure implemented
- Secure password reset mechanism implemented
- Pre-installed device secrets are unique per device and random

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2.9 SDLC, Complementary Measures (C): Vulnerability Handling

- Continuous monitoring of publicly available resources for vulnerability reports
Vulnerability databases as ICS-CERT (US CISA), NVD (US NIST) and CERT-Bund (German BSI) are checked on a daily basis
- Provision of information on vulnerability issues on public SMA website ([LINK](#))
- Coordinated vulnerability handling and responsible disclosure process
Public information available on SMA website ([LINK](#))
- Membership at CERT@VDE ([LINK](#)) for support of coordinated disclosure process

Wiring functional tests if required by para. 15.2.1

N/A

Confirm that the relevant test schedule is attached (tests to be undertaken at time of commissioning).

N/A

Note.

The inverter was tested in a test laboratory. The correct wiring functional test in the field has to be done by the responsible person for the installation of the plant.

Logic Interface (input port) Required by paragraph 11.1.3.1

P

Confirm that an input port is provided and can be used to reduce the Active Power output to zero

Yes

Note. Manufacturer information provided.

Provide high level description of logic interface, e.g. details in 11.1.3.1 such as AC or DC signal

Yes

As shown in the following picture, the communication port B&C are used to logic interface, FS1 port and Vcc port which configured by Users can be operated by an external switch or contactor. When the switch is opened, the inverter will operate normally. When the switch is closed, the inverter will cease to export active power within 5 seconds.

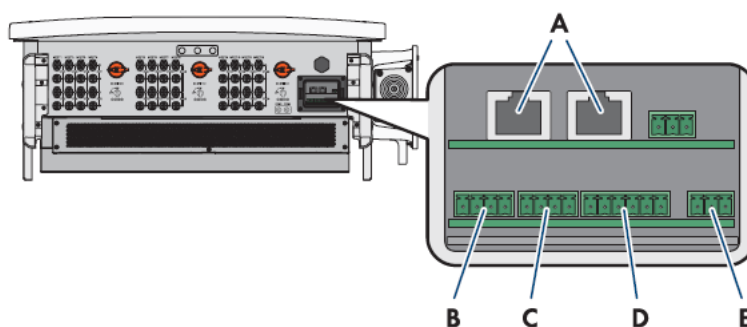


Figure 9: Digital inputs on the COM assembly

Position	Designation
A	Ethernet connections
B	Terminal for fast stop
C	Terminal for fast stop
D	Terminal for digital inputs for curtailment
E	Connection for the multifunction relay

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